Engineered Substrates

Engineered Substrates Using the NanoCleave^{TM} Process

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SiGen Presentation Outline

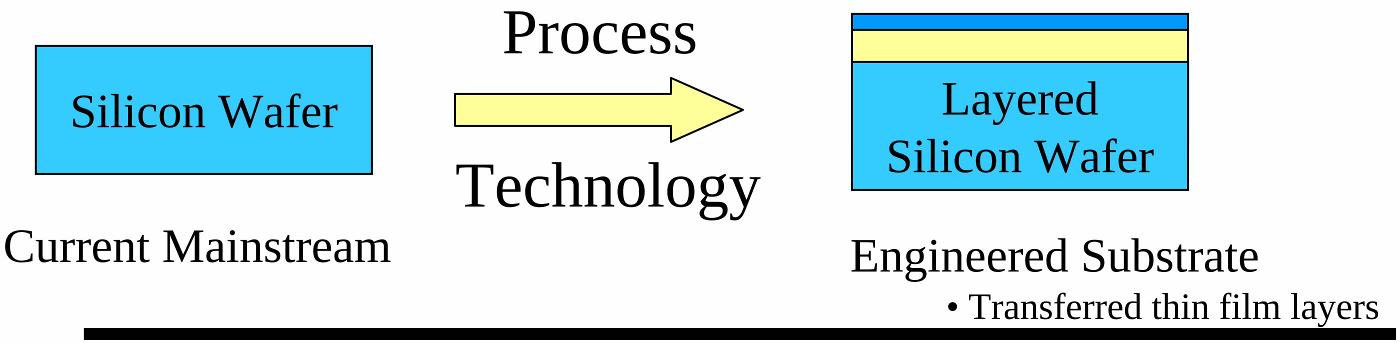
- Engineered Substrates
- Why Layer-Transfer (LT)
- SiGen Layer-Transfer and Bonding Technologies
- Semiconductor Applications
- Packaging Applications
- Display Applications
- Solar Applications
- Conclusions

Demand for High-Performance ICs

High performance ICs and displays are essential in today’s fastest growing next generation products

The Problem: Difficult to meet demand using just device geometry shrinks

The Solution - Engineered Substrates



Silicon Wafer

Current Mainstream

Process

Technology

Layered Silicon Wafer

Engineered Substrate

- Transferred thin film layers

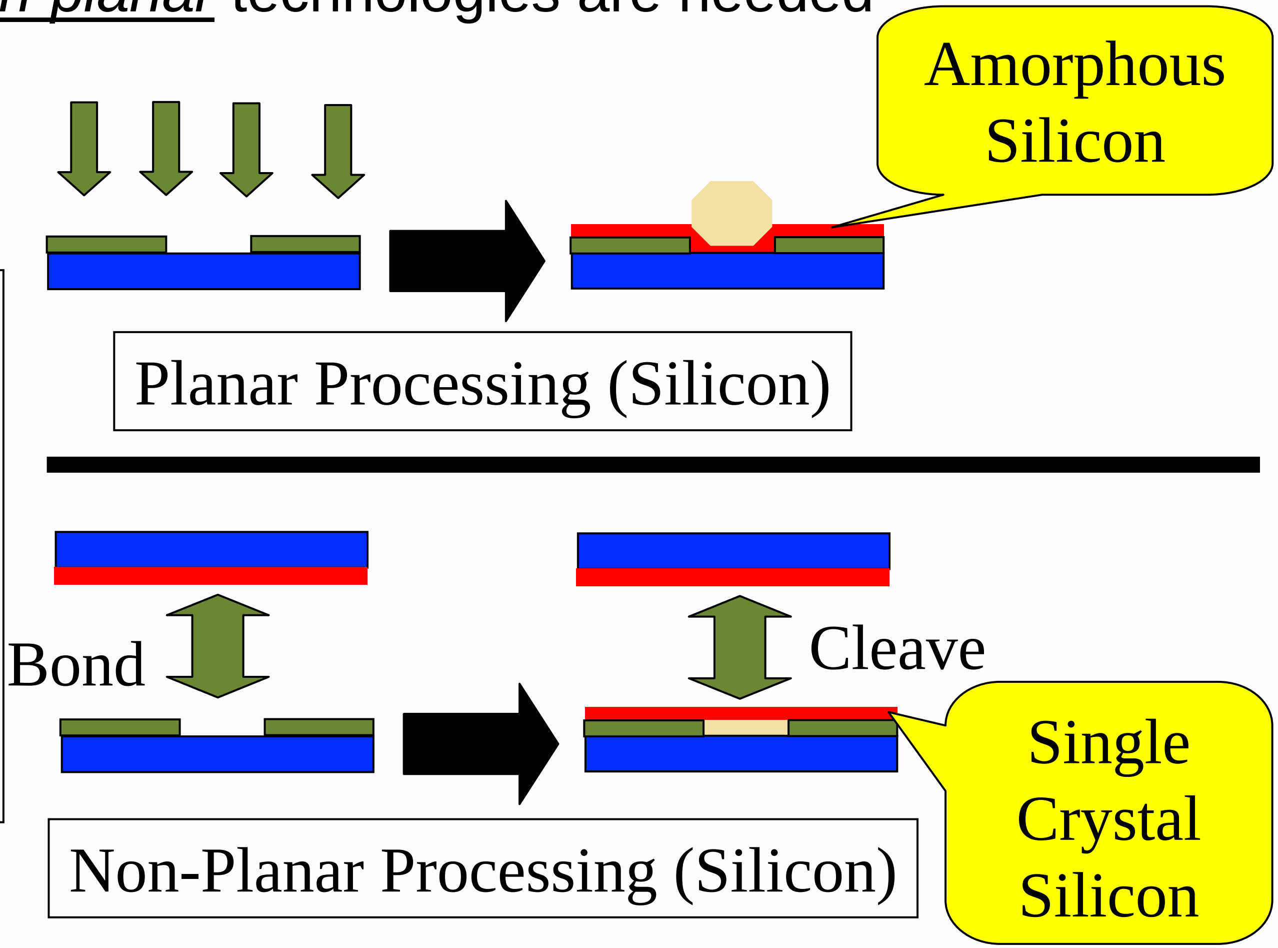
- Engineered Substrates – a "must have" for advanced applications
  - Applications – IC Devices, LCD Displays, 3D Packaging
  - MOSFET leakage reduction => Reduced power dissipation
  - Reduced capacitance => Higher speed and lower power
  - Improved short channel effects => Stable device operation at small size
  - Modification of Materials => Enables new material combinations

Same Geometry – higher performance and lower power using existing manufacturing technology

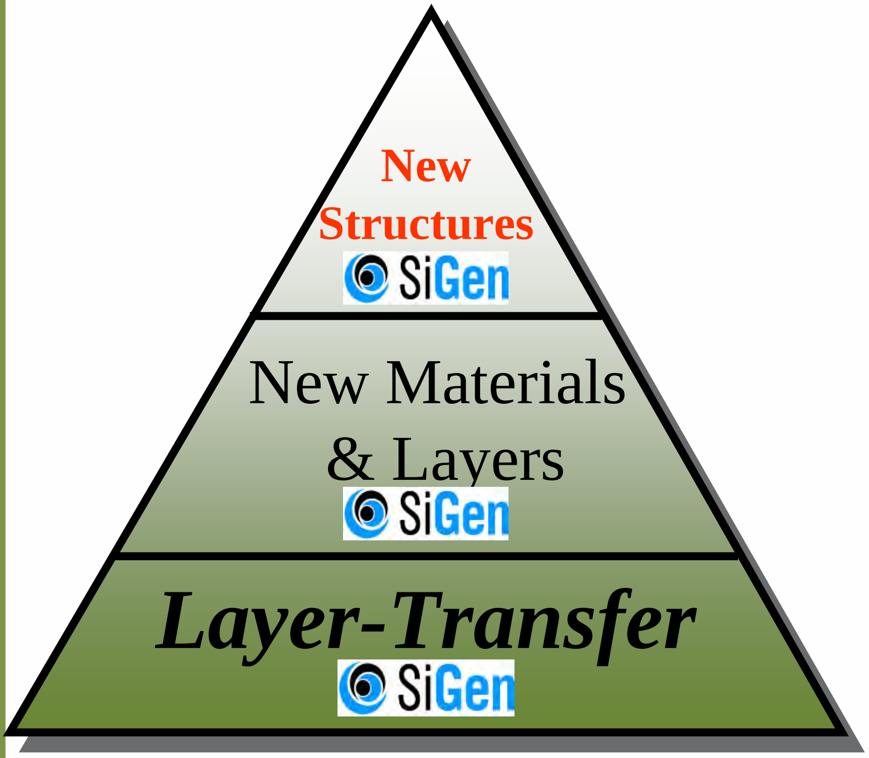
Why Layer-Transfer?

- Most semiconductor layers use *planar* technologies.
- For many of the next-generation engineered substrate applications, *non-planar* technologies are needed

- SOI
- Strained-SOI
- 3D Devices
- FinFET/TriGate
- Cavity Engineering



SiGen Proprietary Technology



New Structures

New Materials & Layers

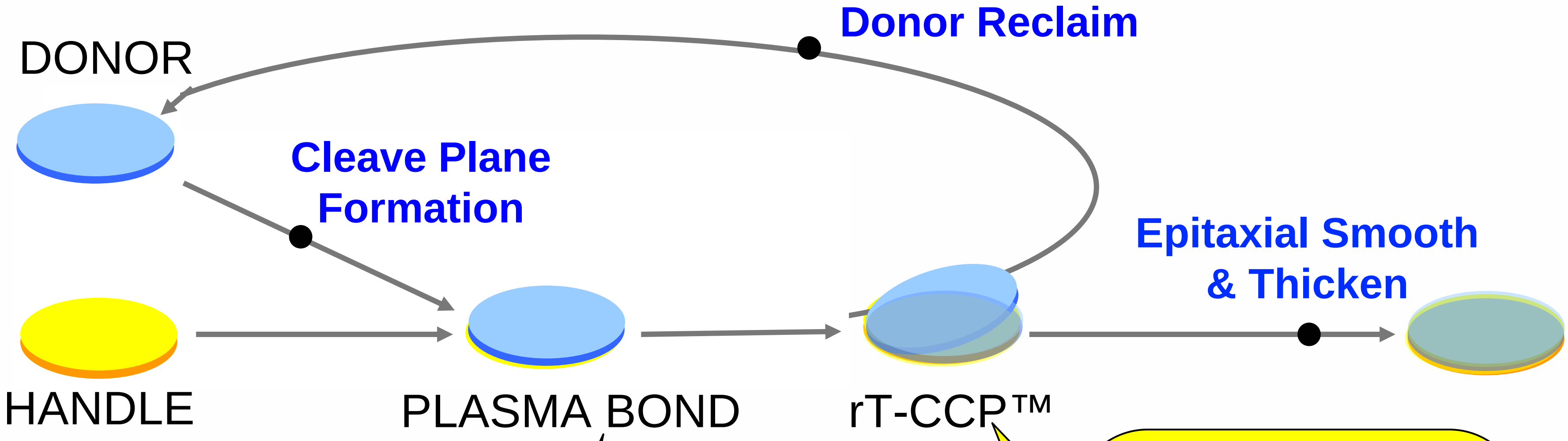
Layer-Transfer

APPLICATIONS

- SOI – high performance semiconductor
- Hybrid Orientations - DSB
- SOQ – Silicon on Quartz – Projection TVs and Displays
- SOG – Silicon on Glass – LCD and Solar
- 3D Packaging
- MEMS

Multiple large markets for SiGen’s patented technology

SiGen NanoCleave™ Layer-Transfer Process



DONOR

Donor Reclaim

Cleave Plane Formation

Epitaxial Smooth & Thicken

HANDLE

PLASMA BOND

rT-CCP™

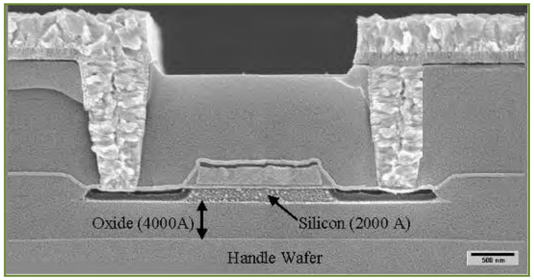
SiGen's patented technology enables the transfer of thin donor layers onto semiconductor or other material substrates

SiGen
Plasma-Activation
and
rT-CCP Tools

Standalone Plasma-Activation Tool

SiGen rT-CCP™ Tool

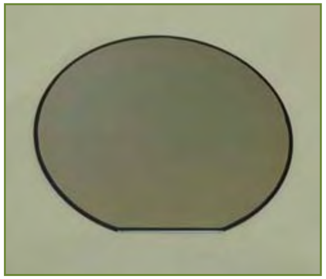
SiGen Key Technologies



- Layer-Transfer
  - Bond Technologies (NanoBond™)
  - NanoCleave™ Layer-Transfer
  - Surface Finishing Technologies (NanoSmooth™)

- Equipment Technologies
  - Plasma-Bond tool technology
  - rT-CCP Cleave tool technology

- New Material Combinations
  - Strained-SOI
  - GeOI
  - SOQ, SOG
  - Solar Cell Technology



Innovation Points

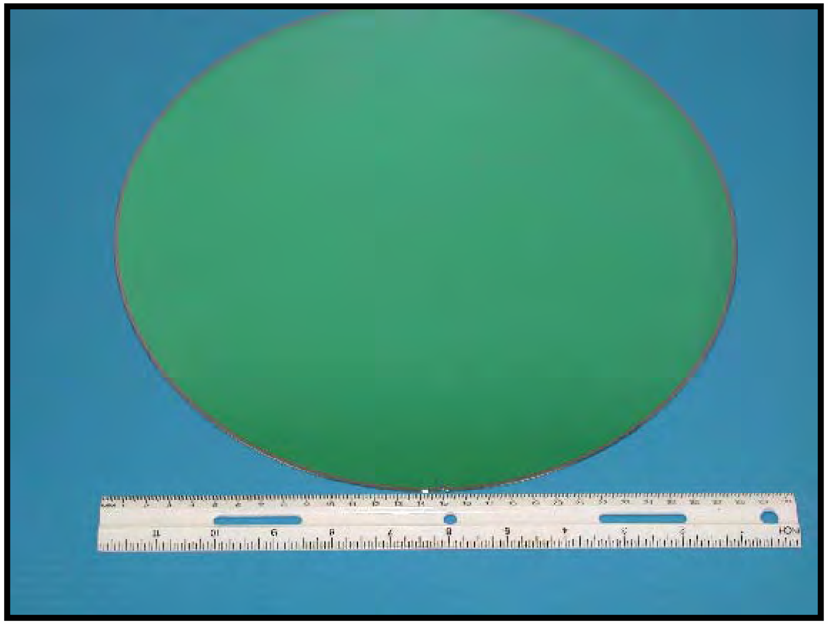
- Cold Process – allows unique dissimilar material systems
- Non-Contact Smoothing – Best Ultra-Thin SOI uniformity
- Plasma-Bonding – Excellent dry fusion bond specifications
  - Wide Applicability in multiple fields
  - Unique In-Situ Bond Technology
- Proven Compatibility
  - With next-generation applications
  - With existing semiconductor process equipment

Allow high-yield and cost-effective formation of 3D, SOI, SOQ, SOG, GeOI, and other material systems

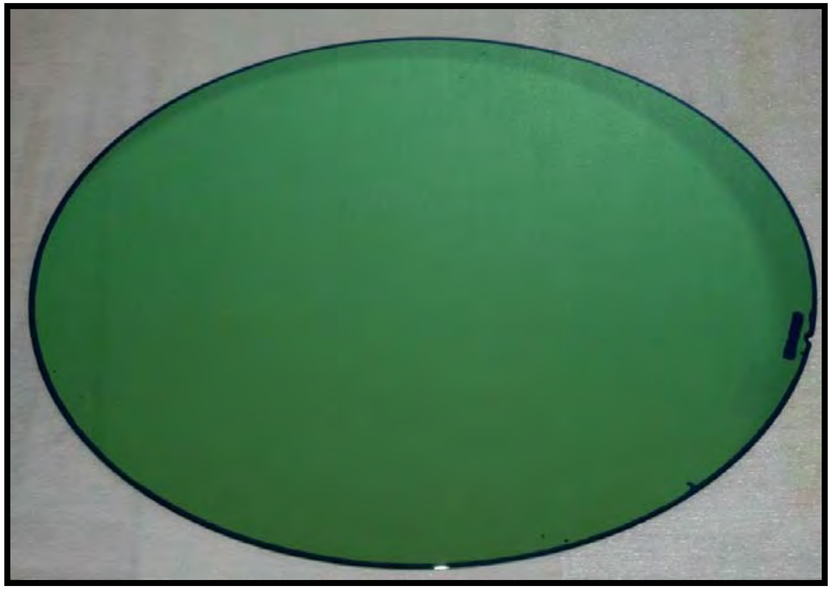
Semiconductor Applications

SOI & Strained-SOI Application

- Multiple Commercial Licenses (MEMC, Others)
- Strained-SOI Demonstrated
- 200mm and 300mm SOI Proven in Production



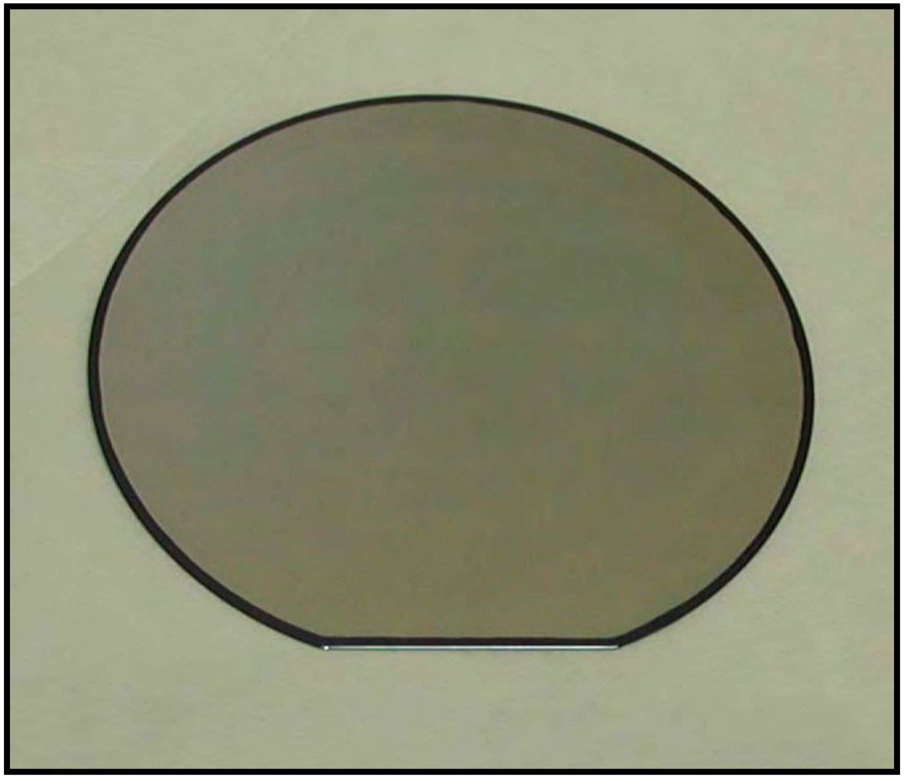
300mm SOI Wafer



Strained-SOI (SSOI)

GeOI Substrate Application

- Silicon Base Substrate
- Single-Crystal Germanium Layer-Transfer
- Low-Temperature Bond and Cleave

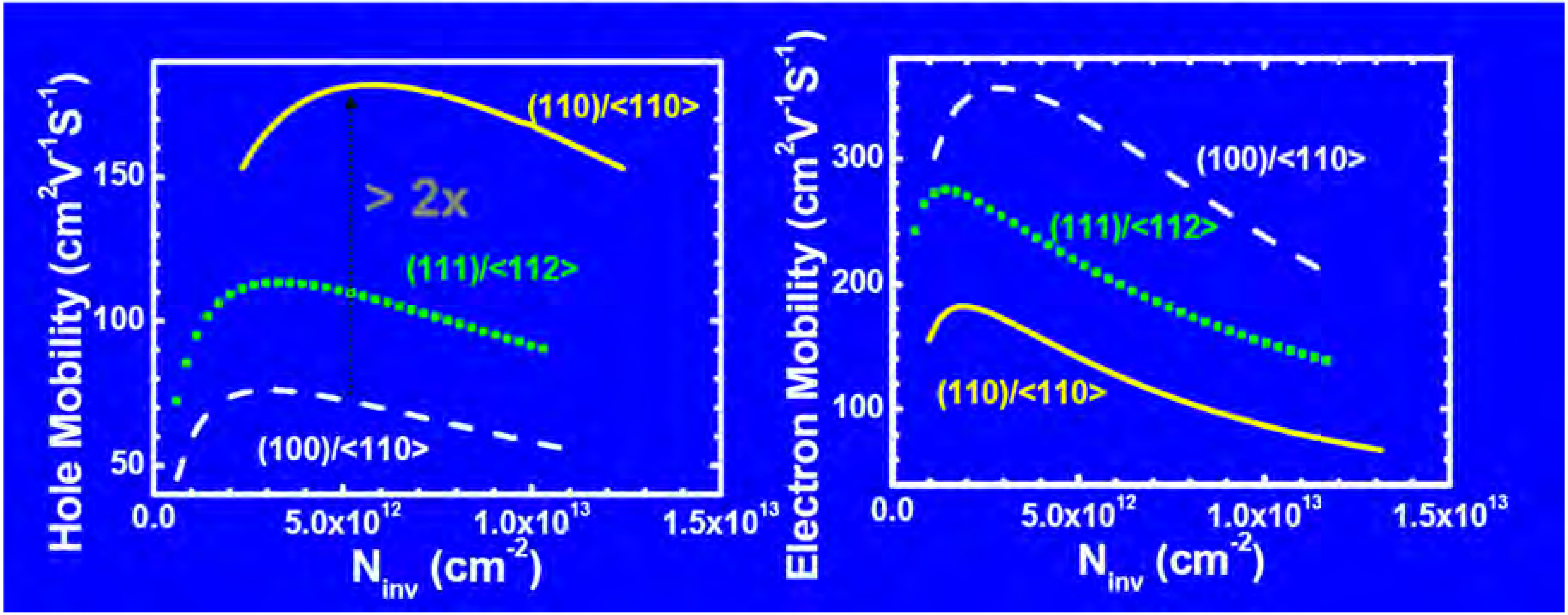


Direct Silicon Bond Opportunity

New Technology: Hybrid Orientation

Combining Highest PMOS and NMOS Mobility

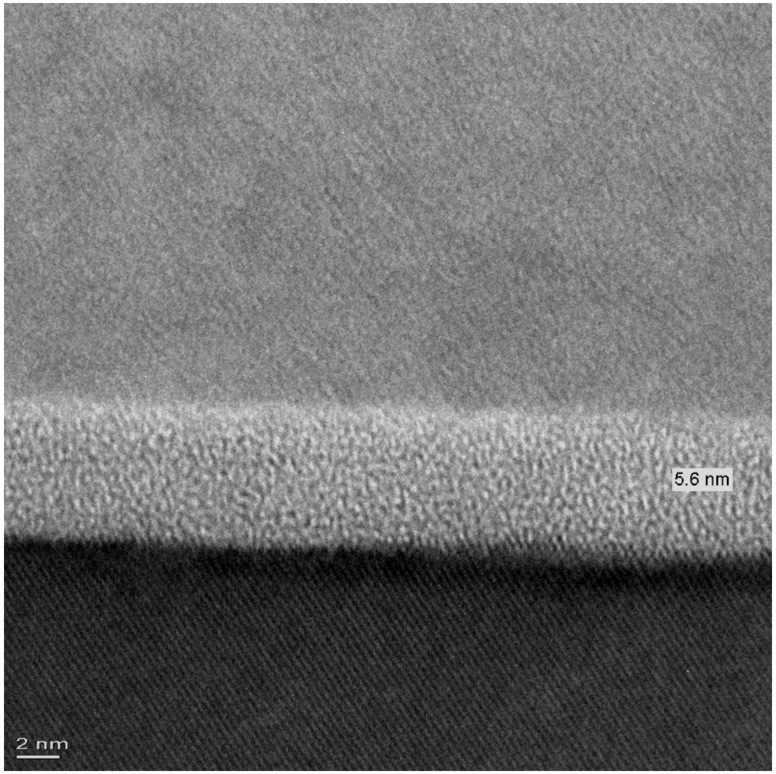
Electron mobility is highest on (100) surface
Hole mobility is highest on (110) surface



Welser, IEEE SVC EDS Seminar June 2005

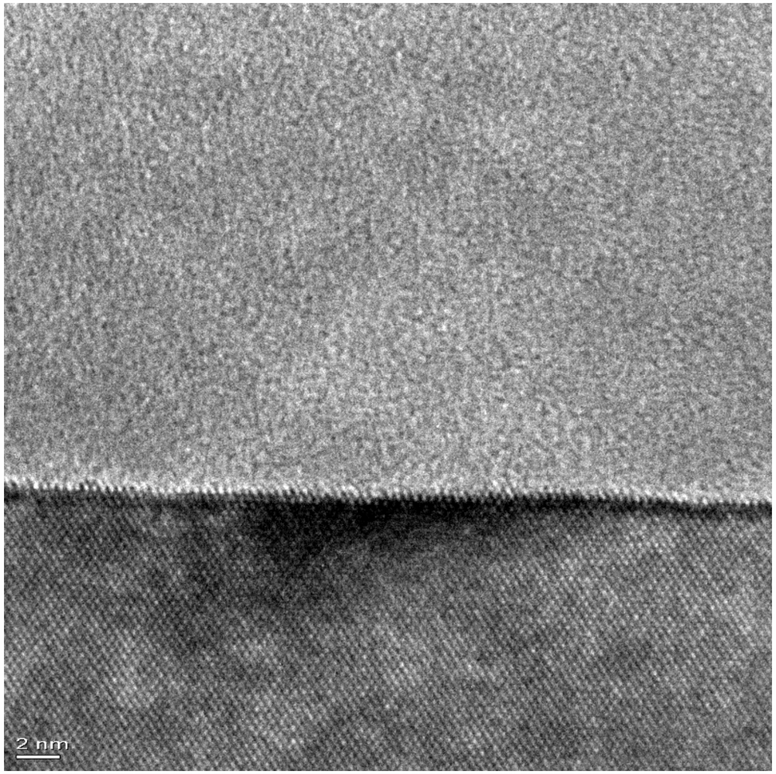
Si-Si Hybrid Orientation Technology

As-cleaved



<110> direction (across and along view)

EPI-Smooth + Anneal

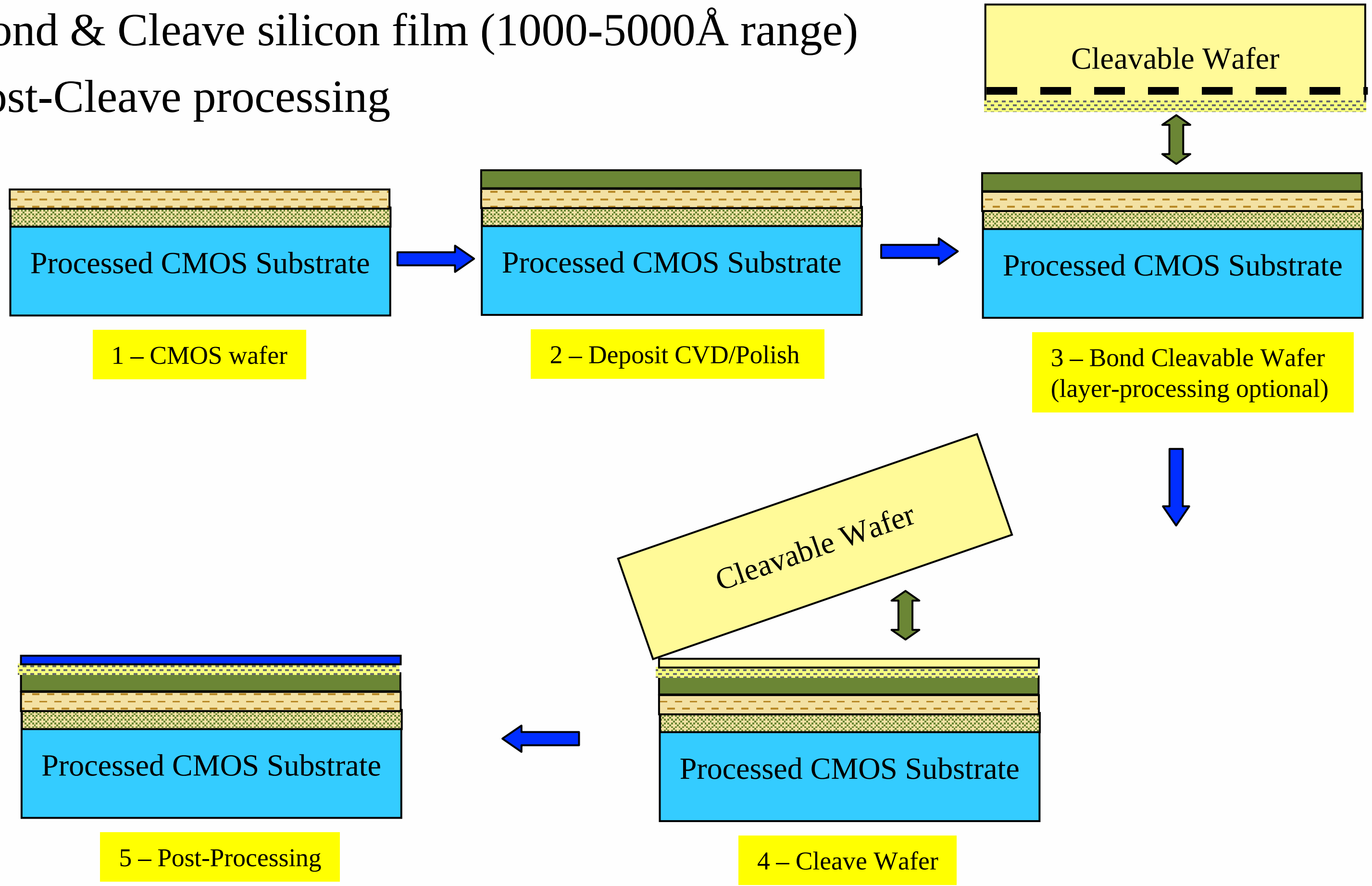


<110> direction (across and along view)

3-D Packaging Opportunity

Stacked CMOS/Device Structures

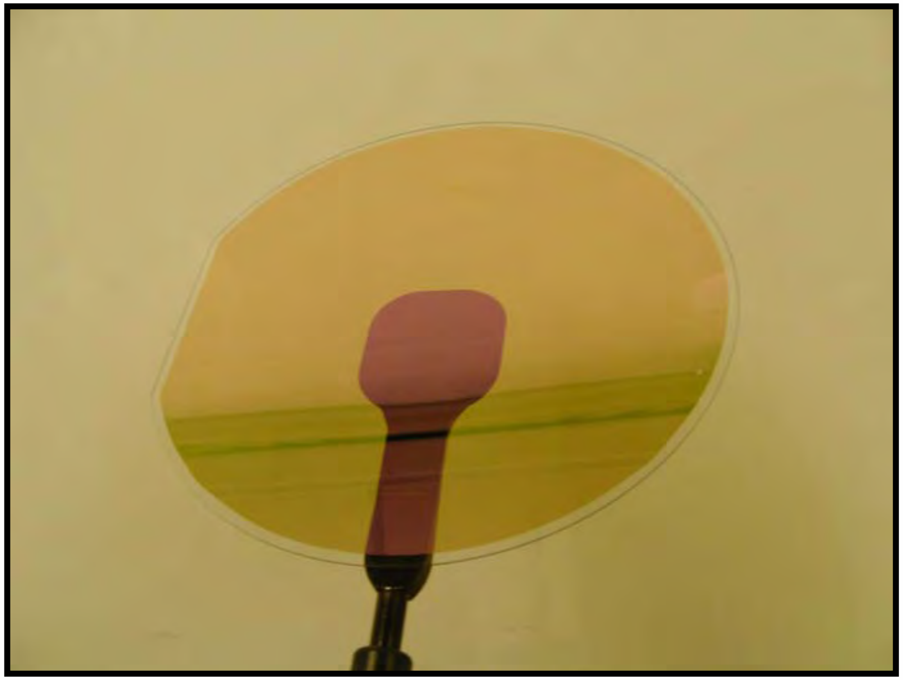
- SiGen layer-transfer can be used for building stacked devices
  - Build CMOS/Device substrate with interconnects
  - Deposit CVD oxide and polish
  - Bond & Cleave silicon film (1000-5000Å range)
  - Post-Cleave processing



SOG/SOQ Flat-Panel Display Opportunity

Silicon-On-Quartz (SOQ) Application:

- Quartz Base Substrate for Optical and RF Applications
- Single-Crystal Silicon Layer
- Higher quality and performance for HDTV Projectors
  - Better brightness
  - Lower Cost
  - Higher Resolution
  - Faster Speed
  - Higher Circuit Density
- Production Ramp



Benefits of cSOG for FPD Applications

- Single Crystal Silicon
  - Higher mobility than amorphous (a-Si) and Low-Temperature Polysilicon (LTPS)
  - Allows high-mobility silicon layers for high-density circuit integration
- High Performance Device Applications
  - Higher bandwidth mobile communication (3G and 4G)
  - Full-motion color video
  - Field sequential addressing with LED or OLED color backlight
  - Fast LC modes (i.e. VAN) important to exploit advantages

Single-Crystal SOG (cSOG) Opportunity

Tri-Color Backlight → Field Sequential LCD → VAN LC Mode →

LED or OLED

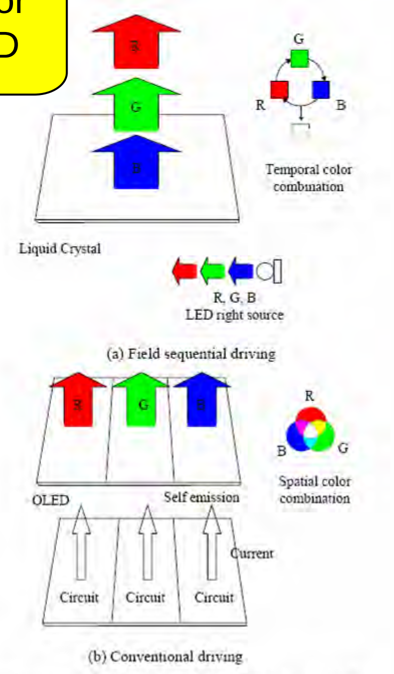
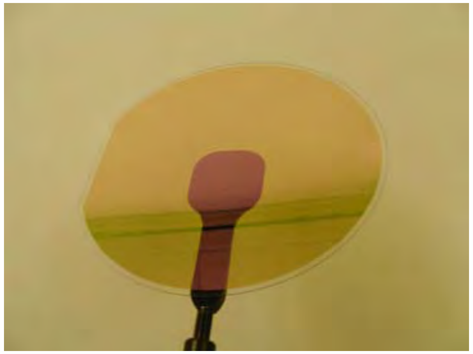


Figure 4 Comparison of pixel driving principle

Source: W.K. Kwak (Samsung SDI) SID 2005



Source: SiGen

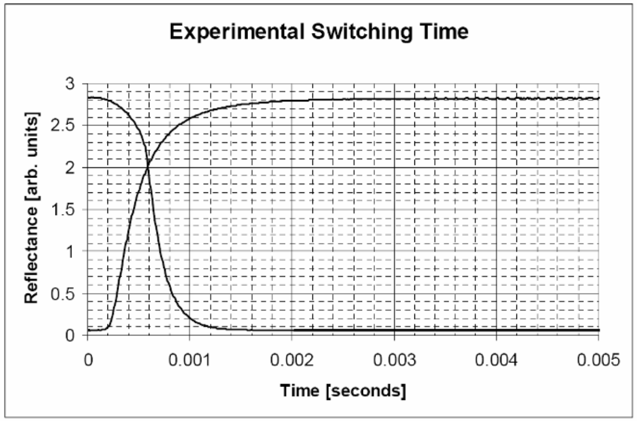
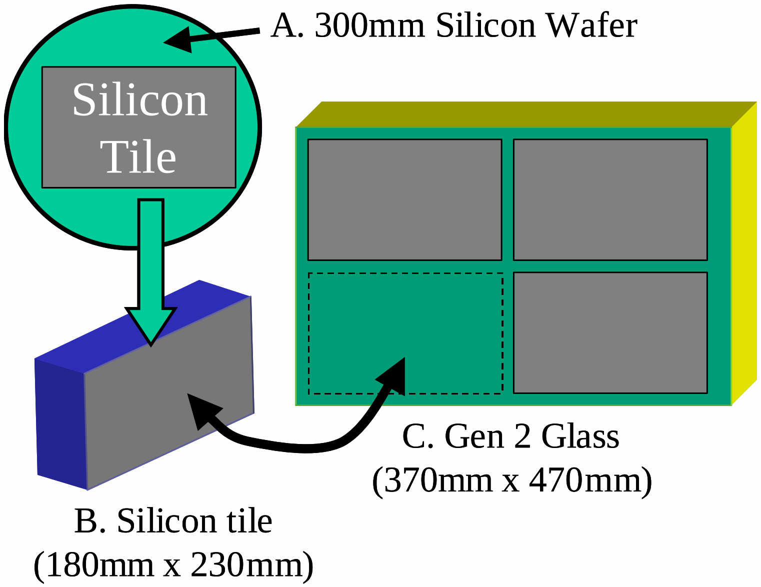


Figure 5. Experimental switching time for fluid 2 at 1.3 µm thickness. The voltages were 5.5V and 0V.

Source: J. Anderson (Hana uDisplay) SID 2005

Large-Area Glass (SOG) Opportunity

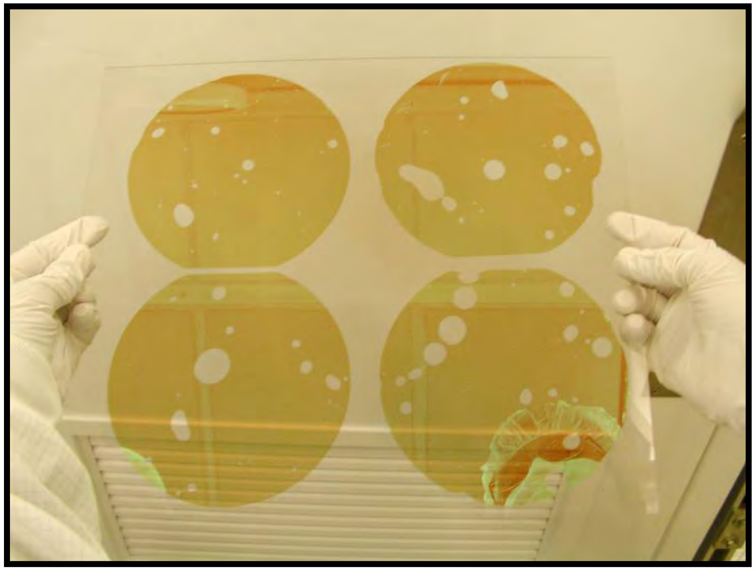


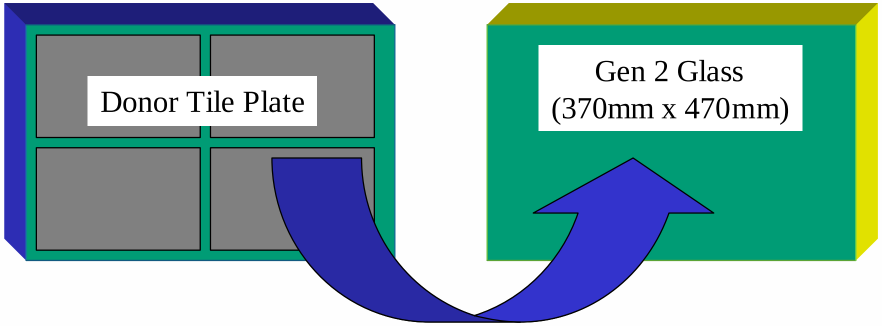
A. 300mm Silicon Wafer

Silicon Tile

B. Silicon tile
(180mm x 230mm)

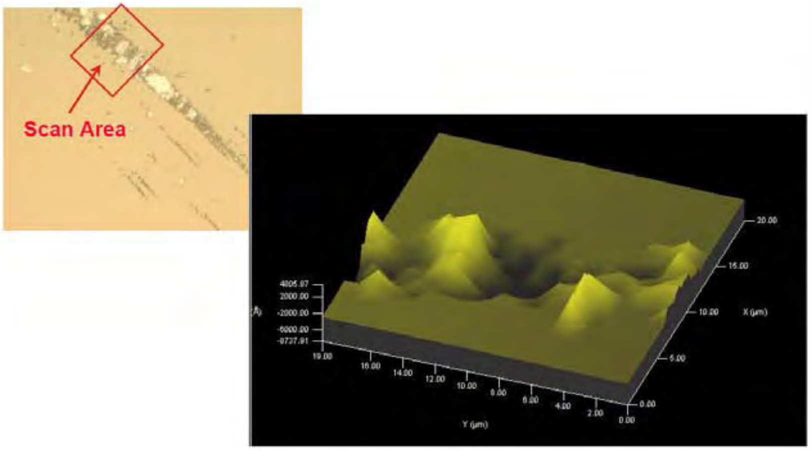
C. Gen 2 Glass
(370mm x 470mm)





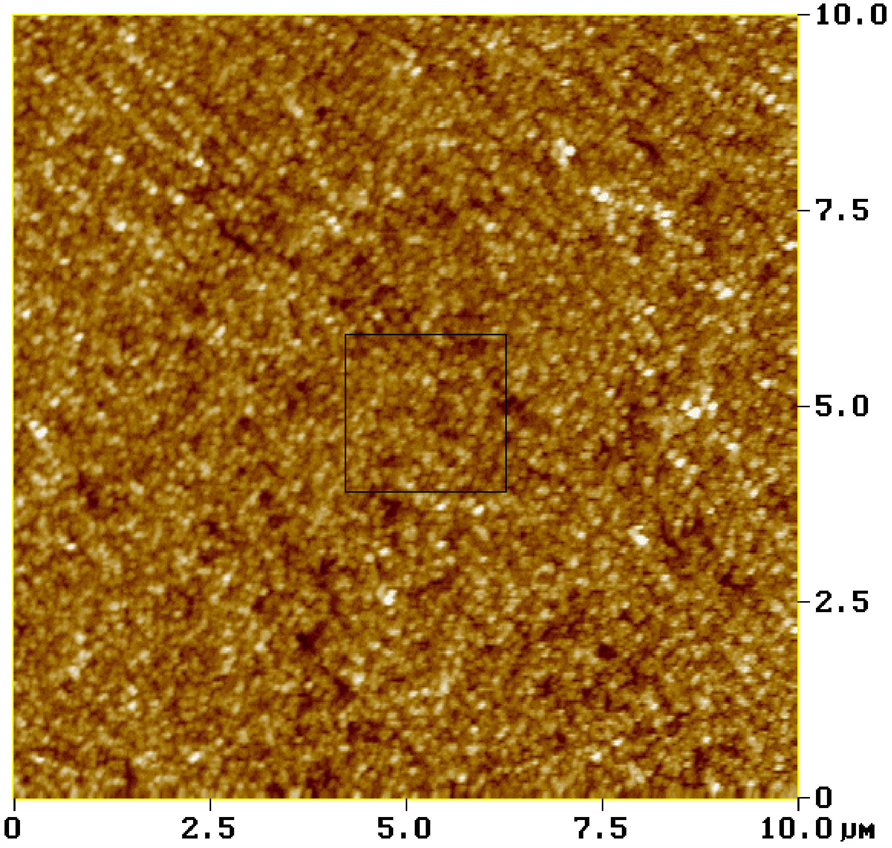
Donor Tile Plate

Gen 2 Glass
(370mm x 470mm)



As-Cleaved c-Si Film Quality

1. Roughness



```
          Image Statistics
 Img. Z range   52.309 nm
 Img. Rms (Rq)  4.378 nm
 Img. Ra        3.400 nm
             Box Statistics
 Z range                   28.973 nm
 Rms (Rq)                  3.901 nm
 Mean roughness (Ra)       3.111 nm
 Skewness                  0.094
 Kurtosis                  2.978
 Line density              7.314 /µm
 Box x dimension           2.070 µm
 Box y dimension           2.031 µm
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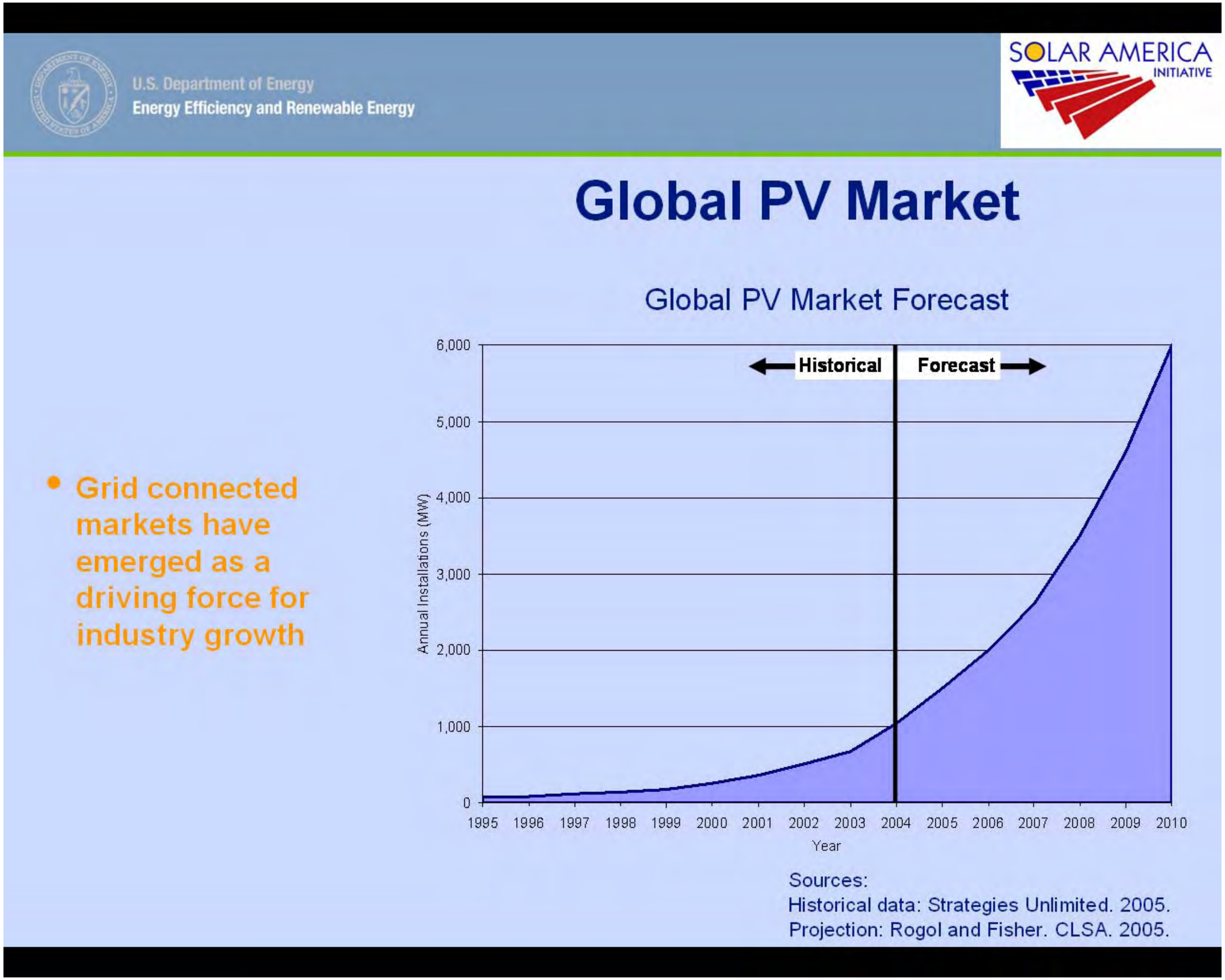
10um x 10um AFM picture of the as-cleaved silicon film showing 43 Å RMS roughness

Solar Cell Opportunity

A Large and Growing Market



U.S. Department of Energy
Energy Efficiency and Renewable Energy

SOLAR AMERICA INITIATIVE

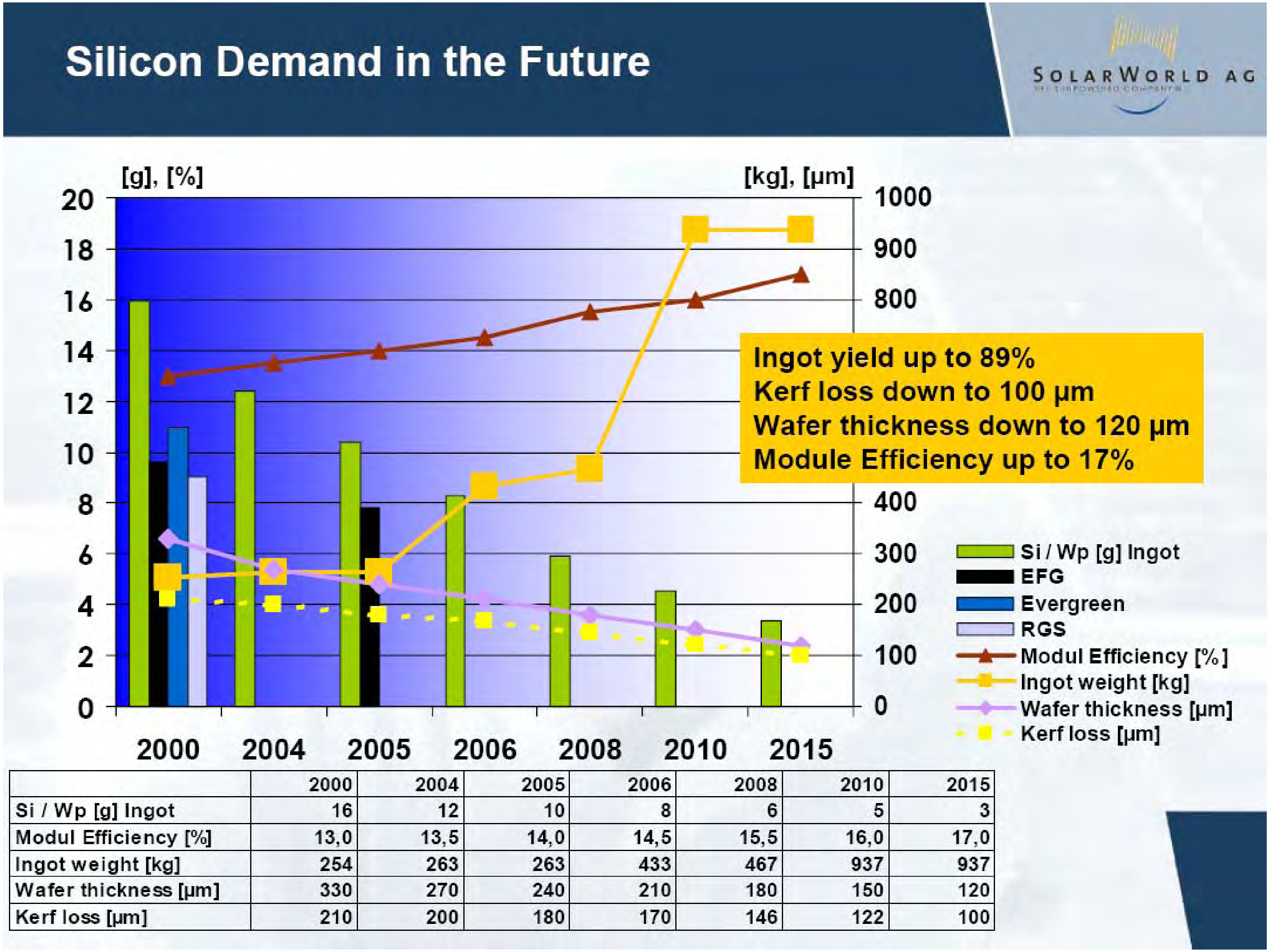
Global PV Market

- Grid connected markets have emerged as a driving force for industry growth

Global PV Market Forecast

Sources:
Historical data: Strategies Unlimited. 2005.
Projection: Rogol and Fisher. CLSA. 2005.

Future Poly-Si Demand Will Keep PV Prices High



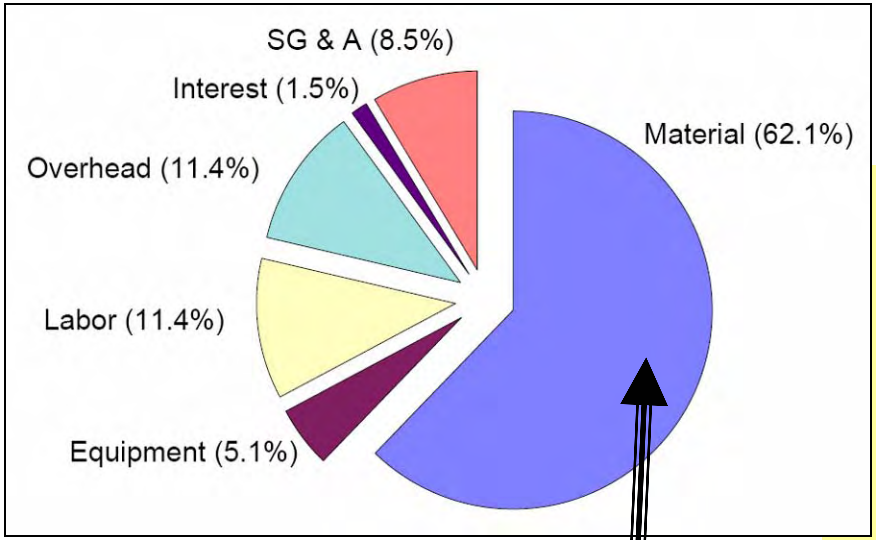
Silicon Demand in the Future

Ingot yield up to 89%
Kerf loss down to 100 µm
Wafer thickness down to 120 µm
Module Efficiency up to 17%

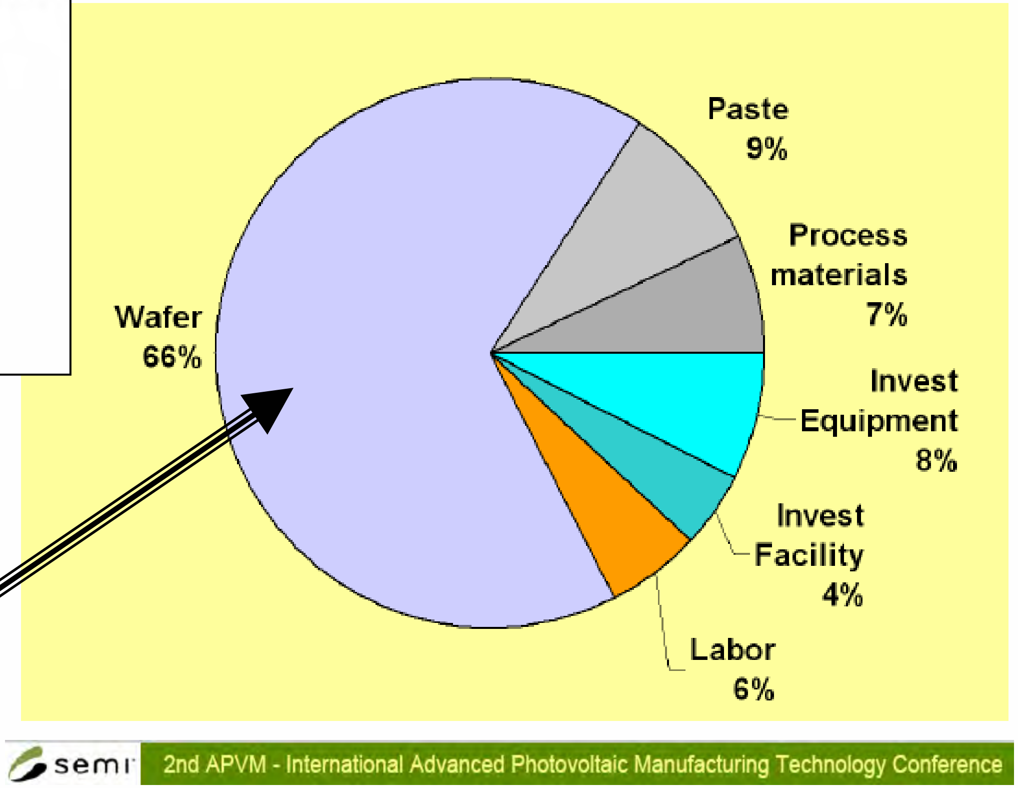
	2000	2004	2005	2006	2008	2010	2015
Si / Wp [g] Ingot	16	12	10	8	6	5	3
Modul Efficiency [%]	13,0	13,5	14,0	14,5	15,5	16,0	17,0
Ingot weight [kg]	254	263	263	433	467	937	937
Wafer thickness [µm]	330	270	240	210	180	150	120
Kerf loss [µm]	210	200	180	170	146	122	100

B. Klebensberger, SolarWorld AG, Semicon Europa 2006

…But Poly-Si is a Major Cost Factor



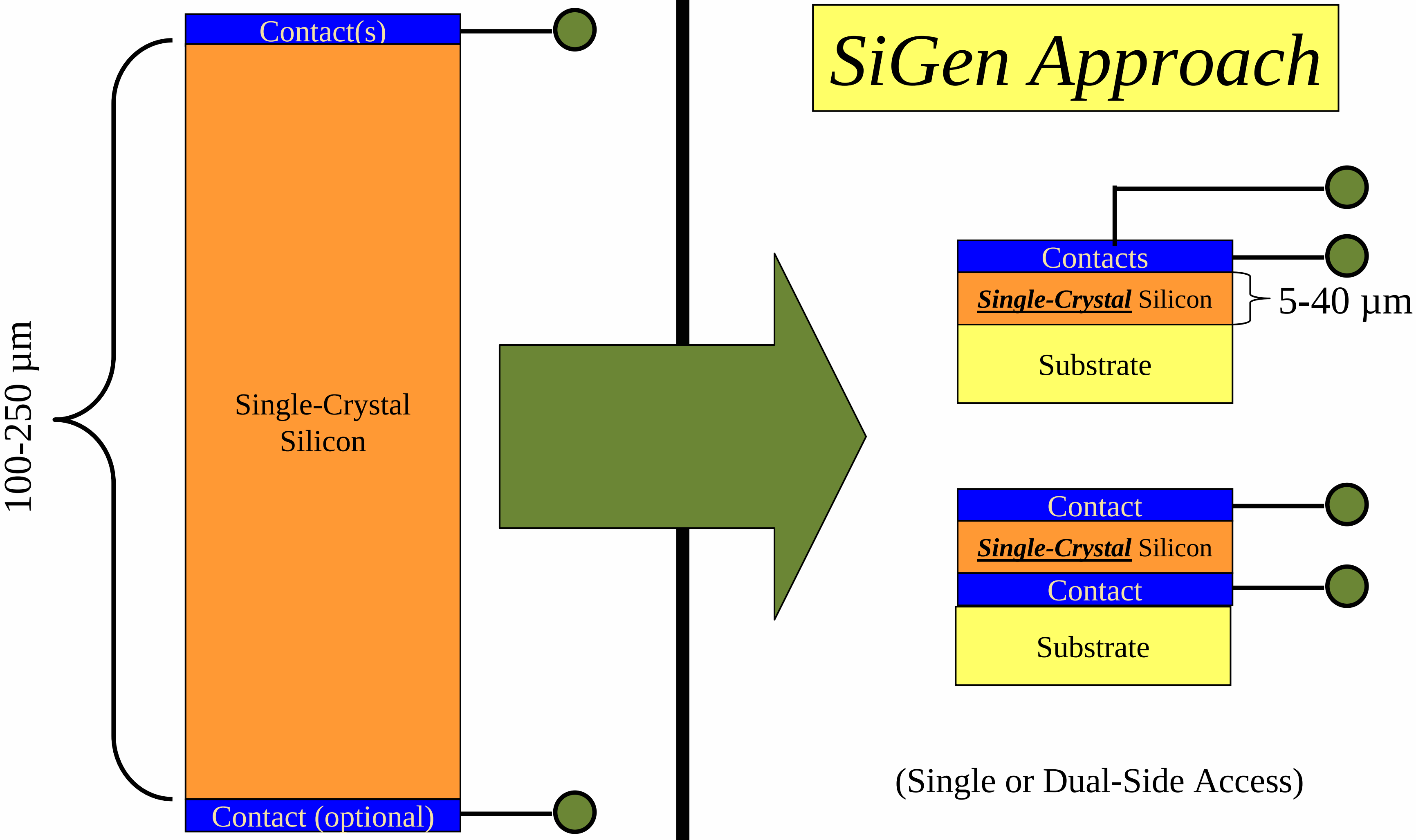
H. Moritz, GT Solar, Semicon Europa 2006



J. Haas, Centrotherm Photovoltaics, Semicon Europa 2006

Silicon Wafer is Major Module Cost Contributor

SiGen Approach: 20X Poly-Si Decrease



A. “Thick” c-Si PV Substrates

Contact(s)

Single-Crystal Silicon

100-250 µm

Contact (optional)

(Dual-Side Access)

B. “Thin” c-Si PV Substrates

SiGen Approach

Contacts

Single-Crystal Silicon

5-40 µm

Substrate

Contact

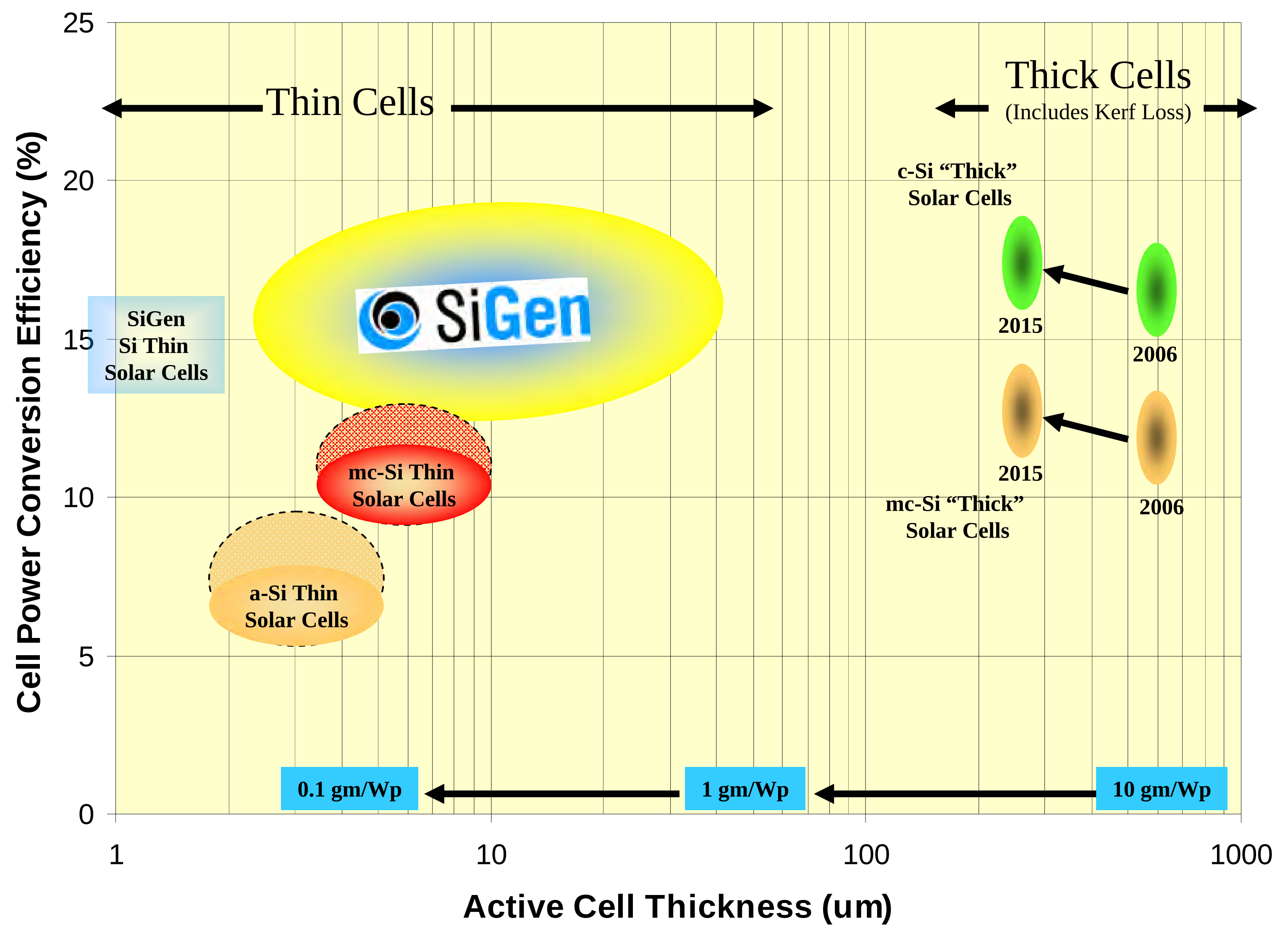
Single-Crystal Silicon

Contact

Substrate

(Single or Dual-Side Access)

SiGen Solar Cell Positioning



Conclusions

- Engineered substrates open up new markets with new applications
- Layer-transfer offers a cost-effective process to achieve many variations of highly engineered films
- SiGen’s processes and HVM tools are proven solutions in the semiconductor and display industries
- Packaging, solar, and opto-electronics offer new opportunities