23rd European Photovoltaic Conference
Conference Preprint
2BO.2.3

DIRECT FILM TRANSFER (DFT) TECHNOLOGY FOR KERF-FREE SILICON WAFERING

F. Henley, A. Lamm, S. Kang, Z. Liu and L. Tian
Silicon Genesis Corporation, 61 Daggett Drive, San Jose, California 95134 USA

ABSTRACT: A new beam-induced large-area crystalline silicon PV wafering process with near zero kerf-loss has been developed. This paper introduces the Direct Film Transfer (DFT) process and describes its practical utilization to slice thin (50-150μm) PV wafers in high-volume manufacturing. The material characteristics such as lifetime, mechanical strength and TTV when monocrystalline silicon ingots are wafered using this new process are also summarized and show excellent results compared to traditional multi-wire slurry saw (MWSS) slicing methods.
Keywords: Substrates, c-Si, Manufacturing and Processing, DFT, Wafering, Sawing

1 INTRODUCTION

In wafered silicon PV systems, key cost areas are use of relatively thick silicon slices, high kerf loss and relative scarcity of the silicon absorber material. One solution to improve silicon use efficiency is thin-film deposition but practical approaches suffer from substantially lower conversion efficiency. Another solution presents itself by combining advanced layer-transfer cleaving methods with efficient, high-energy ion accelerator technology. The convergence of these two technologies allows a thickness of silicon made from a CZ silicon ingot to be directly detached using a high-energy light ion beam with near-zero kerf loss and with low overall process cost. The process is called Direct Film Transfer (DFT) and shown conceptually in Figure 1. Equipment and wafers using the DFT process will be called by the trade name PolyMax™.

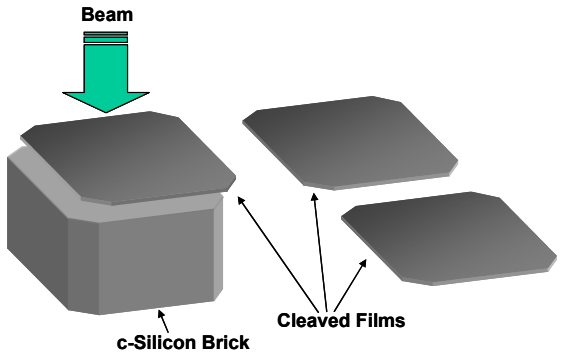

Figure 1: DFT Wafering Concept

The DFT process eliminates many of the wafering process steps while allowing substantially thinner and low-kerf silicon thicknesses to be realized. The result is a cost and manufacturing complexity reduction. Compared to the sawing process, the DFT process is also less taxing on the environment due to (i) less overall energy is consumed since the slurry-rich sawing/wafering processes are eliminated, (ii) the use of CZ silicon and polysilicon stock are substantially reduced (energy intensive steps themselves), and (iii) no use or production of slurry, saw wire and kerf loss material.

2 PROCESS & EQUIPMENT DESCRIPTION

Using elements of a hydrogen-assisted cleaving principle first demonstrated in the early 1980s by Russian researchers [1,2], the DFT process is a 2-step (implant-cleave), dry slicing technology that operates to convert squared monocrystalline silicon ingots or bricks of about 5-10 cm thickness into PV wafers. The first step is to form a cleaving plane at the desired thickness under the brick face using high-energy hydrogen (proton) beam irradiation. The incident mono-energetic protons lose their energy as they traverse a silicon thickness to form a stressed End-Of-Range (EOR) layer. In silicon, 2-4MeV proton energy is required to form a cleave layer at the desired 50-150μm wafering thickness.

Proton accelerator technologies have become more commercialized and efficient due to technology advances and market drivers such as proton cancer therapy, manufacture of radio-isotopes and homeland security. For example, accelerators using compact RF-quadrupole (RFQ) technologies are now entering commercial use.

One major design consideration is the need to effectively manage the substantial heat generated by the implant process. To avoid overheating the brick surfaces and achieve practical manufacturing throughput rates, a tray with multiple bricks assembled in an array was adopted along with fast electro-magnetic scanning. The tray is about 1m x 1m in area with a 6x6 array size for 156mm wafers and 8x8 array size for 125mm wafers. The trays are cycled between the implant and cleave subsystems in a flexible factory material flow approach. More details of the configuration and design of the manufacturing system are presented elsewhere [3]. The tray configuration and fast scanning inherently provides the means of developing patterned dose and thermal profiles across each brick, a key element of the high productivity cleaving process.

Once the cleave plane is developed, the tray is moved to a cleaving subsystem that uses a 2-step initiation-propagation sequence to cleave the wafer from each brick. A small (mm^2 to cm^2) area has a higher dose that is thermally pulse treated to initiate a starting crack. This crack occurs at an edge area of the cleave plane and is designed to avoid generating cleave artifacts. A second scanning energy source is used to propagate the cleave front from this small initiation area through the brick to fully detach the film. Figure 2 shows the initiation-propagation cleaving sequence using a corner initiation area. The key technology in achieving high throughput is the development and use of advanced controlled propagation to limit the cleave plane dose requirement. The mechanical configuration is challenging since, as opposed to bonded layer-transfer configurations using double cantilever beam geometries, thin-film release on a thick brick donor can generate substantial in-plane shear stress intensity components (K_{II}). External energy is used to control the propagation and keep the film from branching out of the cleave plane. Although all major crystal orientations have been experimentally verified,

(111) orientation is the preferred material for DFT use due to its lower surface energy.

Figure 3 shows the equipment concept with the accelerator/end-station implant (Accel-ES) and controlled-cleave module (CCM) making up the 2-step wafering process within a factory environment.

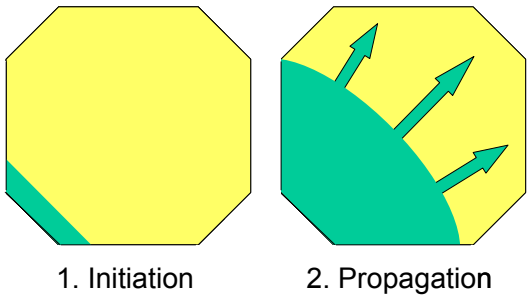

Figure 2: Controlled propagation 2-step sequence on a pseudo-square brick

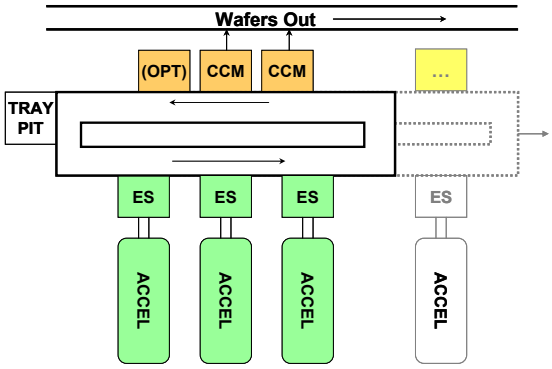

Figure 3: Production System Factory Layout

3 DFT WAFER MATERIAL CHARACTERISTICS

The mechanical, electrical and functional characteristics of PolyMax™ wafered silicon were evaluated. The DFT process has been experimentally used to produce films spanning from thin-film to free-standing wafer substitutes. Large-area CZ silicon films of 17µm, 50µm, and 120µm thickness have been produced. One example is a 50µm, 125mm pseudo-square wafer as shown in Figure 4. A 50-150 µm wafering range is planned for the first PolyMax™ equipment set.

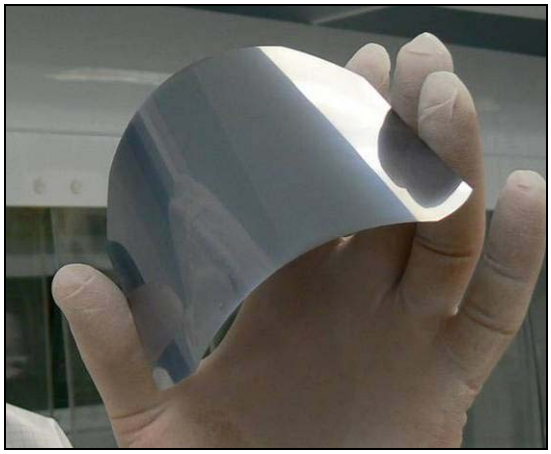

Figure 4: PolyMax™ 50µm thick 125mm wafer

3.1 MECHANICAL

Preliminary data regarding surface roughness, TTV, edge, and mechanical strength using this technology are very promising.

Roughness of the cleaved film is generally much less than 1µm and proportional to cleave thickness. Figure 5 shows AFM of a 50µm PolyMax™ film compared to a 240µm wiresaw reference wafer. The excellent surface roughness of the process is apparent.

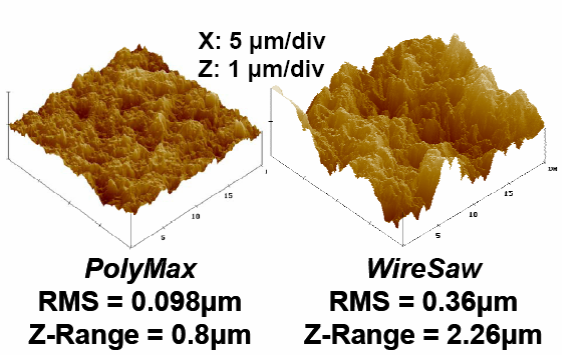

Figure 5: AFM surface roughness comparison – PolyMax™ and wiresaw wafers (20µm x 20µm scale)

TTV is less than 1-2% and SEM microphotographs show excellent edge quality (Figure 6 & 7). The comparison of PolyMax™ side and edge profiles to conventional wiresaw processed wafers demonstrates its substantially better dimensional control and edge quality. It is interesting to note that assuming 160µm kerf loss for the wiresawed wafer, the total wiresaw wafer pitch is 400µm versus 50µm for the PolyMax™ wafer, making it fully 8x more efficient in polysilicon feedstock use.

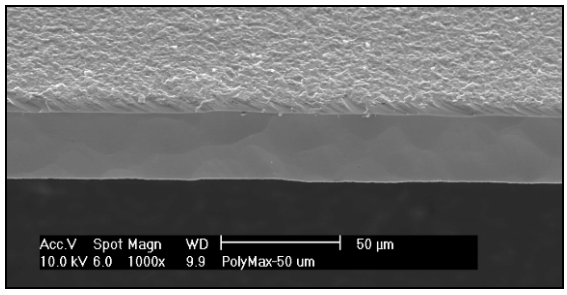

Figure 6a: 50µm PolyMax™ wafer side profile (50µm scale)

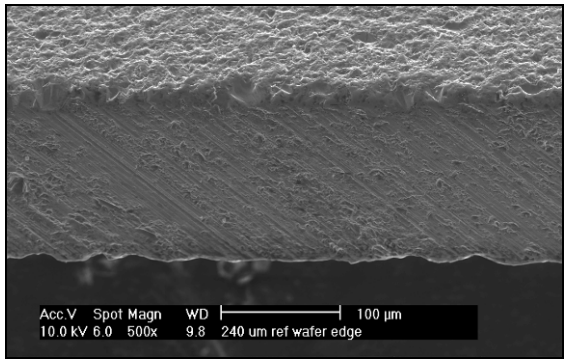

Figure 6b: 240µm wiresaw wafer side profile (100 µm scale)

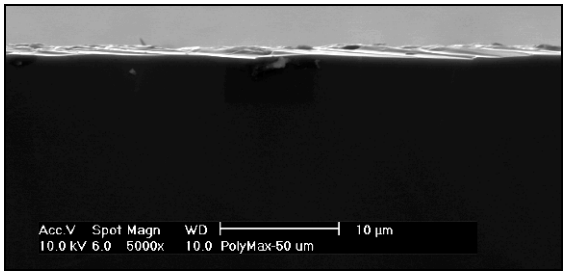

Figure 7a: PolyMax™ wafer edge profile (10 µm scale)

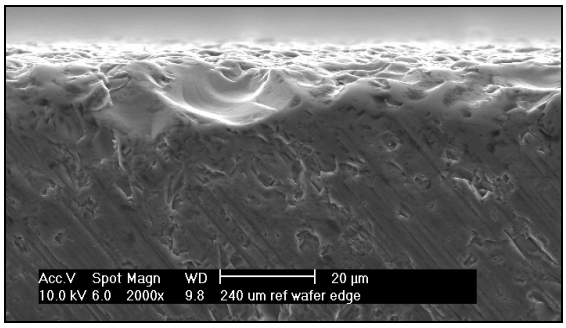

Figure 7b: 240µm wiresaw wafer edge profile (20 µm scale)

One unexpected benefit from the DFT process sequence was the measurement of surprisingly high mechanical strength of the resulting wafers. This is believed to be a result of the lower defect generation rate of the implant-cleave slicing method. Table I shows the results of ring-on-ring stress to fracture mechanical tests on 50µm PolyMax™ samples compared to 240µm using ring-on-ring. An etch of 7µm per side improved surface stress to breakage from an already impressive 1.5 GPa to 2.4 GPa. Interestingly, many (111) triangular samples showed fracture stress over 10 and even 20 GPa. In contrast, the wiresaw reference samples consistently yielded substantially lower strength due to crack injection during the sawing process [6, 7]. Figure 6 & 7 SEM microphotographs show the cleaner and less defective process result.

Table I: Stress-to-fracture mechanical strength test (Ring-on-Ring, 9mm/4mm ring sizes, 10.5mm square samples diced from 125mm wafers)

	As-Sliced	Post-Etched (Δ ~ 14µm)
PolyMax™ 50µm	1500 MPa	2400 MPa
240µm Wiresaw Reference	98 MPa	310 MPa

The process has also been verified to be capable of repeatedly detaching films from a brick without surface preparation between successive detachments. The films continue to have similar roughness and Total Thickness Variation (TTV) without any interim polishing or other surface modification steps. This suggests that the process can be scaled to high-volume, low-cost manufacturing with minimal surface reconditioning.

3.2 LIFETIME RECOVERY AND MEASUREMENT

Minority carrier lifetime degradation by high-energy proton irradiation is a well known and researched phenomenon due to the importance of solar cells in space applications [4, 5]. A main element of developing the DFT process was therefore linked to demonstrating minority carrier lifetime recovery. Effects such as contaminant co-implantation are also of concern but careful implant system design can mitigate this issue.

A radiation damage production and annihilation model was developed and showed that specific DFT implant process sequences could eliminate extended defect production. Using implant temperature control to limit radiation damage density and recognizing that only the End-of-Range layer must be removed as a damage layer, a post-cleave "etch/anneal recovery" was found to work well in recovering high bulk minority carrier lifetime. It was found that using these sequences, most of the lifetime degradation were limited to divacancy (V-V) radiation damage production that can be readily corrected using post-cleave annealing. Normal cell processing would be more than sufficient to develop the lifetime anneal required and thus the step is considered an inherent part of the cell process. The End-of-Range layer etch can be done at the "saw damage etch" step within the solar cell process.

PolyMax™ wafers can thus be fully lifetime recovered simply by running the wafer through a normal cell process sequence that includes a surface etch and an anneal/drive-in.

Minority carrier lifetime on 50µm PolyMax™ wafers were measured by a photoconductance tester and shows over 300µsec at MCD 1E+15 cm^{-3} lifetime using a single-step etch/anneal recovery process. Table II also shows how lifetime improves with increasing surface etch. A 50µm polished CZ reference wafer was also measured. Note that these measurements are uncorrected for surface recombination velocity. As a result, the bulk lifetime may be substantially higher than reported.

Table II: Sinton Consulting WCT-120 effective lifetime measurements of PolyMax™ wafers with "etch/anneal recovery". Anneal was a single 850C/3minute treatment.

	Thickness (µm)	Lifetime (µsec) * (MCD=1x10^{15} cm^{-3})
As-Cleaved	47	<10
Etch #1	39	100
Etch #2	37	160
Single-Step Recovery	35	350
Polished CZ Reference	50	250

* Uncorrected for surface recombination velocity

3.3 PV CELL FABRICATION AND MEASUREMENT

To show end product functionality, PV test cells were made in collaboration with Georgia Institute of Technology's Center of Excellence for Photovoltaics. A slightly modified cell process was used to fabricate 4 cm^2 PV cells on p-type 50µm, 6 Ω-cm PolyMax™ and 275µm, 3 Ω-cm CZ reference wafers. Both had lifetime of at least 100µsec. The cells were made using a ~78 nm

silicon nitride coated front-side with an n+ 0.5-1 µm thick, 35 ohm/□ emitter. The back surface was a CVD deposited Al film ~1 µm thick. The process was not optimized for the thin substrates but showed basic functionality.

Figure 8 shows the I-V curves of 4 cm^2 cells yielding 13.2% and 14.6% conversion efficiency respectively. The efficiency difference was bridged between the reference and the PolyMax™ cell by using PC-1D and changing only resistivity and thickness. The 1.4% efficiency difference can therefore be fully accounted by the PolyMax™ material's higher resistivity and 40µm thickness. Use of texturization on a more advanced cell design is in planning.

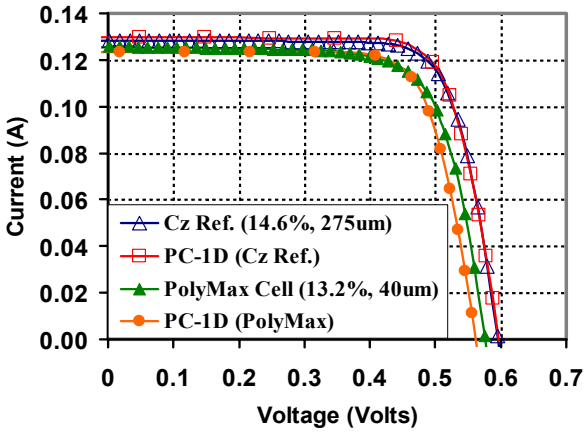

Figure 8: PolyMax™ and CZ reference cell efficiency test

4 EQUIPMENT THROUGHPUT AND EFFICIENCY

An equipment set is currently under design to perform the PolyMax™ process in high-volume manufacturing. The equipment is expected to produce about 5-7MW equivalent of wafers per year with an energy cost of about 0.6kW-hr/Wp produced (150µm wafer thickness). This compares favorably with multi-wire slurry saw (MWSS) systems if the slurry and satellite systems such as washing/drying and singulation systems are included. If the kerf-loss savings are also included, the system can become a net energy saving step over the incumbent sawing method.

5 CONCLUSION

A novel kerf-free, dry wafering process has been introduced and described. Called Direct Film Transfer (DFT) or PolyMax™, the process uses a 2-step implant-cleave method where high-energy light ion irradiation first forms a cleave plane followed by advanced controlled cleaving to initiate and controllably propagate a fracture plane along the cleave plane to release a large-area wafer from a shaped ingot.

The process has been used to produce test samples to show material quality, characteristics and demonstrate scaling to high-volume manufacturing. Surface roughness, edge quality, mechanical strength, lifetime and test cell efficiency results confirm the viability of the method as a PV wafering technology with excellent conversion efficiency with low polysilicon feedstock use.

The economic impact and applicability of a practical kerf-free PV wafering process with high material quality is substantial. The process can be used to fabricate free-standing substrates of 50µm to 150µm for substitutive and advanced wafer PV manufacturing. The process also shows potential to make high-quality ultra-thin films of 20-50µm thickness.

This wide thickness range allows the process to participate in both the "thin" and "thick" silicon PV markets. For thick "free-standing" substrate manufacturing processes, the process allows less expensive absorber at equivalent efficiencies. For thin absorbers, the ability of the process to generate 20-50µm thick high-efficiency silicon absorber films, possibly mounted onto large mechanical backing material satisfies a novel form factor that has been challenging for the industry to achieve. The technology can ultimately offer a high lifetime and efficiency alternative to current thin-film technologies.

REFERENCES

[1] V. F. Reutov and Sh. Sh. Ibragimov, Method for fabricating thin silicon wafers, *USSR Inventor's Certificate No. 1282757*, December 30 1983

[2] B.N. Mukashev & al., Hydrogen Implantation into Silicon, phys. stat. sol. (a) **91**, 509 (1985)

[3] F. Henley & al., Kerf-Free Silicon Wafering Equipment Configurations Using Beam-Induced Cleave Technology, 23rd European Photovoltaic Solar Energy Conference visual presentation 2DV.1.68 (2008)

[4] M. Yamaguchi & al., High-energy and high-fluence proton irradiation effects in silicon solar cells, J. Appl. Phys. **80** (9), 4916 (1996)

[5] A. Hallen & al., Lifetime in proton irradiated silicon, J. Appl. Phys. **79** (8), 3906 (1996)

[6] K. Wasmer & al., Effect of Strength Test Methods on Silicon Wafer Strength Measurements, Proceeding of the 22rd European Photovoltaic Solar Energy Conference, paper 2CV.3.20 (2007)

[7] A. Bidiville & al., Towards the Correlation of Mechanical Properties and Sawing Parameters of Silicon Wafers, Proceeding of the 22rd European Photovoltaic Solar Energy Conference, paper 2CV.3.19 (2007)