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KERF-FREE SILICON WAFERING EQUIPMENT CONFIGURATIONS USING BEAM-INDUCED CLEAVE TECHNOLOGY

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ABSTRACT: A new ion beam-induced cleaving process for slicing wafers with near zero kerf-loss has been developed and demonstrated to be production-worthy on full size substrates. This paper introduces the manufacturing equipment and a modular, scalable factory architecture that will implement this new process for high-volume manufacturing.
Keywords: Substrates, c-Si, Manufacturing and Processing, DFT, wafering, sawing

1 INTRODUCTION

Rapidly growing demand for clean photovoltaic energy sources has led recently to an intense focus on reducing the cost of PV cell manufacturing. It is widely recognized in the PV industry that achieving so-called 'grid-parity' will require significant reductions in cost per watt. Simultaneously, the high demand for photovoltaics has dramatically increased the price of polysilicon feedstock material. These cost pressures are driving the industry to use ever-thinner wafers in order to reduce the quantity of silicon material.

Figure 1 illustrates the typical historic development of wafer thickness and kerf-loss as well as an example forecast for the future. The new kerf-free wafering technology is also included for comparison. Presently the industry is distributed between 160 and 200 um wafer thickness and a similar range of variation in kerf-loss. There is also an interest to evaluate sub-100 um thickness for advanced PV manufacturers for future production lines. Furthermore, R&D results show that sub-50um high-efficiency cells are possible using high-quality silicon absorber material.

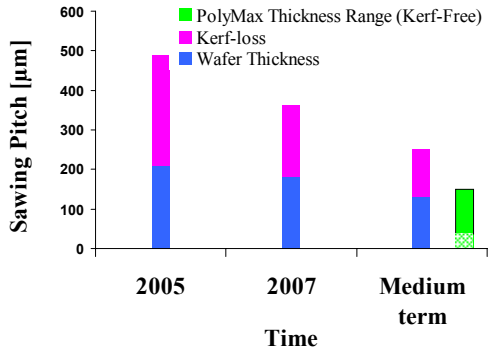

Figure 1: Historic development of wafer thickness and kerf-loss including a possible medium term scenario.

The current wafer slicing technology, wire sawing with a silicon carbide slurry represents both a high share of the wafer manufacturing cost and also a barrier to further major reductions in kerf-loss.

This paper introduces a new type of wafering equipment and factory architecture that performs the novel Direct Film Transfer (DFT) process described elsewhere in this conference [1]. Unlike wire-sawn wafers, the new DFT wafers suffer virtually zero kerf loss, thereby reducing the quantity of silicon consumed per wafer by roughly half. The range of typical DFT wafer thicknesses is also show in fig. 1.

While the difference in silicon consumption is striking, DFT wafering also has other cost and performance advantages described below that, together with the savings in silicon, provides the potential to make the DFT wafering a key enabler in overcoming economic and technical barriers to widespread PV commercialization.

2 WIRE SAWING LIMITATIONS

At present, all commercial wafering of monocrystalline silicon (cz-Si) and multicrystalline silicon (mc-Si) for PV cells is done using wire saws [2, 3]. In wire sawing, a fine steel wire is drawn across the surface of a squared silicon ingot or brick at high speed. The wire entrains a slurry of lubricating coolant and silicon carbide abrasive into the cut, gradually abrading the silicon. In production wire-sawing equipment the wire is wound many times around a set of spinning mandrels forming an array of hundreds of parallel equally spaced wires, allowing the saw to cut several thousand wafers simultaneously.

The most glaring drawback of wire sawing is a problem inherent to all sawing processes: the kerf-loss. Valuable silicon from the cut is abraded to a powder form and mixed with the abrasive slurry. Figure 1 shows that for wire-sawn wafers the kerf currently consumes about half of the overall silicon brick. While some of the lost silicon may be recovered from the slurry, the process of recycling continues to be technically challenging and unresolved on a cost efficient basis.

In addition, thin wire sawn wafers tend to be fragile and suffer yield losses due to the damage introduced into the wafer surface by the abrasive sawing processes. Furthermore, there is substantial wafer-to-wafer thickness variation and within-wafer thickness variation.

In order to not have the kerf consume an ever larger fraction of the starting material, scaling of wire saw technology also requires reductions in wire diameter and abrasive grit size. The further scaling down of both the wafer thickness and the kerf is expected to be more difficult and costly than in the past and is likely to limit the rate at which PV costs can be reduced.

3 DFT PROCESS

The DFT process is described in greater detail elsewhere in this conference [1]. Briefly, the process consists of two main steps. The first step is implantation, in which the surface of a brick of cz-Si is exposed to an energetic beam of light ions such as hydrogen. The ions

come to rest in a thin layer at a well-defined depth below the surface of the silicon. This cleave layer establishes a plane along which a fracture, subsequently introduced into the silicon crystal, will preferentially propagate.

The second key step of the DFT process is the actual cleaving of the silicon. The cleaving step consists of a proprietary thermally driven treatment of the brick whereby a fracture is initiated, and caused to propagate along the cleave layer, separating the thin upper layer of silicon from the remainder of the brick. For films more than a few tens of microns thick, the resulting film will be a monolithic, self-supporting wafer. The wafer is removed and the two-step DFT process is repeated on the newly exposed surface of the brick, each cycle producing a single wafer.

Since DFT wafers are formed by a cleaving process rather than sawing, they do not have any appreciable kerf-loss. In addition, since the thickness of a DFT wafer is determined by the highly repeatable physical process of mono-energetic ions stopping at the same depth, the variations in thickness are much lower than for wire-sawn wafers. Finally, the absence of saw-induced surface damage means the DFT wafer tends to be stronger and less prone to breakage enabling high yields in high volume automated production lines.

4 FACTORY ARCHITECTURE

Figure 2 shows a factory layout for a complete DFT wafering system. The two main process steps described above, implantation and cleaving, are each performed in separate process modules labeled (1) and (2), respectively.

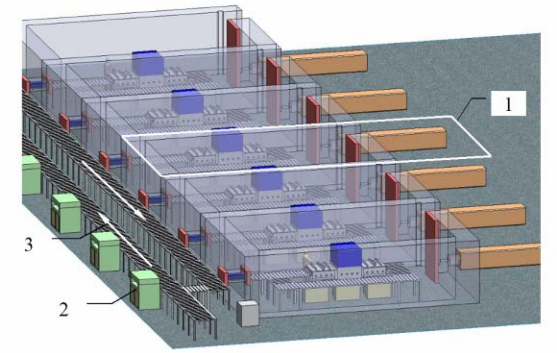

Figure 2: Factory layout showing key system level components: (1) Implant subsystem, (2) cleave subsystem, (3) main factory conveyor loop. Arrows indicate flow of material pallets.

The layout in Fig. 2 includes six implant modules and six cleave modules arranged on either side of a main conveyor (3) that circulates pallets of silicon bricks in a loop (arrows), cycling the pallets between the implant and cleave subsystems.

Wafers released in the cleave module are immediately ready for QC inspection, after which they may be coin-stacked and boxed, or optionally output to a wafer conveyor (not shown) feeding a PV cell production line. Costly wet processes and the related equipment are completely eliminated. These include slurry production, slurry removal, glue dissolving, wafer singulation, wafer washing/drying, and slurry recycling.

This architecture is modular, flexible and scalable. For example, it enables the production line to easily be balanced for maximum efficiency. The ratio of implant modules to cleave modules will ultimately be chosen so that the throughput of the two process steps are roughly equal, and with the more costly implanter as the bottleneck. Parallel operation of multiple implant and cleave modules clearly allows the system to scale smoothly from a single implanter pilot line to production rates in the hundreds of megawatts per year required for high-volume cell manufacturing.

The present design also anticipates that additional process operations may be required. Such operations might include machine vision inspection of the brick surface for quality control, or perhaps periodic brick surface reconditioning. The modular approach allows additional modules for such steps to be easily integrated into the line as needed.

The shaping of the incoming silicon prior to wafering is almost identical to the process used in wire sawing: a boule or ingot of cz-Si is diamond-sawn and ground to form square or pseudo-square bricks. The wafering equipment described here can process bricks up to 100 mm thick depending on various process parameters. Interchangeable process kits will allow the system to handle either 156x156mm or 125x125mm bricks. The bricks are seated in the pallet in an array of 6x6 (for 156x156mm bricks), or 8x8 (for 125x125mm bricks). The throughput of each implant/cleave module pair is expected to range from 180 to 300 wafers per hour depending on wafer form factor, equivalent to about 4 sq. m per hour PV wafer surface production.

A modular control system architecture mirrors the physical architecture of the system. A system controller will control the main conveyor. It will route and track pallets going to and from the various process modules and will dispatch a process recipe associated with each pallet to the target module. Once a pallet is handed off, individual module controllers in each process module will handle the local machine control tasks. The system controller is also responsible for communication with the factory management and automation system.

5 EQUIPMENT DESIGN

Figure 3 shows selected details of the implant module. A key element of the implanter is a high current, high energy ion beam accelerator (1). The accelerator produces a mono-energetic beam of protons or other light ions at energies of a few MeV. The top surface of each of the bricks is exposed to the ion beam inside a high vacuum target chamber (2). Pallets of bricks are admitted to the target chamber through a vacuum load lock (3) and exit the vacuum system via a second load lock (4). The target chamber and load locks are arranged in an inline configuration for maximum throughput with the pallets being supported and moved from chamber to chamber on rollers. The three vacuum chambers are isolated from each other and from atmosphere by large area slit valves.

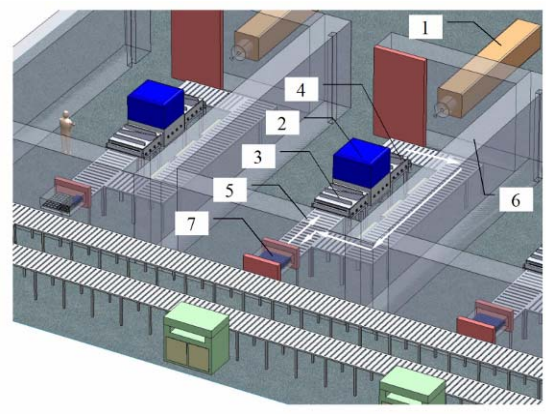

Figure 3: Detail of implant subsystem components: (1) ion accelerator, (2) process chamber, (3) input load lock, (4) output load lock, (5) implant conveyor, (6) shielding enclosure, (7) pallet entry

During treatment by the ion beam, ions will penetrate the surface of the silicon and stop in a thin layer at a depth determined by the well-established theory of the stopping of charged particles in matter. For example, 4.0 MeV hydrogen ions will stop at a depth of 150 microns in silicon.

The equipment described here is designed to be able to produce wafers ranging from 150 microns down to 50 microns thick, depending on the specific hardware configuration. Future versions of the system may allow scaling to as low as 20 microns.

An important consideration in the design relates to brick cooling. The ion beam deceleration process deposits a large amount of thermal energy near the top surface of the brick. To remove this heat, a water-cooled platen located inside the target chamber engages the bottom surfaces of the bricks and extracts the heat by conduction. Also key to managing the heat load is the spreading of the beam power over the roughly 1 m^2 area of silicon on the pallet. The close spacing of bricks on the pallet minimizes the amount of valuable beam current lost to the interstices between bricks. Additionally, the large area of the pallet relative to its perimeter minimizes the beam current lost to over-scan, resulting in a beam utilization efficiency exceeding 80%.

Another important design consideration is control of radiation. The interaction of the energetic ions with the silicon target produces a substantial flux of high energy x-rays (gamma rays) which must be attenuated to safe levels by a shield vault (6) in Fig. 3. Pallets enter and exit the shield vault through a 'radiation lock' (7) penetrating the shield and sealed on each end by a pair of sliding lead doors. Once inside the shield, pallets are transported to and from the vacuum load locks on implant conveyor (5) as shown by the arrows. An aisle is provided adjacent to the vacuum chambers for easy access during servicing.

6 CONCLUSION

The DFT process has been successfully demonstrated on industry standard 125 mm wafers down to thickness as low as 50 microns. This novel process is supported by an advanced equipment set and a factory architecture design for high volume manufacturing of high efficiency cz-Si solar cells.

DFT wafering has the potential for notable advantages over conventional wire sawing; advantages which will grow ever more apparent as the industry moves to thinner wafers. Even at current thicknesses, the elimination of the kerf reduces usage of valuable polysilicon feedstock by half along with a corresponding reduction of front-end silicon process equipment such as crystal pullers, cropping and bricking systems. Enabling the PV industry to scale to sub-100 micron wafers will enable even more efficient use of silicon. Tighter control over wafer thickness and higher material strength will increase yields at both the cell and module level. Together these advantages will drive down the cost per watt and accelerate adoption of PV as an economically viable source of clean energy.

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